SEMICONDUCTOR INTEGRATED ELECTRONIC DEVICE AND CORRESPONDING MANUFACTURING METHOD

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a divisional application of U.S. Application No.

5   10/199,964 filed July 18, 2002, now allowed, which claims priority from European Application Nos. 01830486.5 filed July 19, 2001 and 01127923.9 filed November 23, 2001, all three of these applications being incorporated herein by reference in their entireties.

Field of Invention

10   The present invention relates to an electronic device which is integrated in a semiconductor substrate. More particularly, it relates to a structure of an electronic device that can be integrated monolithically in a semiconductor, e.g., a FET (Field-Effect Transistor).

The invention further relates to an integrated memory circuit

15   comprising a plurality of such transistors. The invention is directed to increase the number of memory cells that are integrated in the semiconductor material, and improve the quality of the information that is stored in the memory.

BACKGROUND OF THE INVENTION

20   Current technologies for fabricating semiconductor integrated devices have led to a large reduction in the circuit area requirements of individual electronic devices. In the case of a FET, this is achieved by progressively reducing the size of the FET active areas that compose the basic blocks of most electronic circuits. Sub-micron size (e.g., 0.18-micron) transistors can be currently obtained,

25   and the scaling-down trend shows no signs that it may end there with the integration process.

All types of semiconductor circuits have benefited from the intensified integration, and especially so integrated memory circuits having non-volatile memory cells, such as EPROM, EEPROM and Flash-EEPROM cells, integrated therein.

5   There are two types of non-volatile memories which are comprised of floating-gate transistors. The first type is represented by EPROMs and can be programmed electrically and erased optically.

The second type, represented by EEPROMs and Flash-EEPROMs, allows the stored information to be modified electrically for both writing and

10   erasing.

In either cases, the information is recorded in the memory in the form of electric charges that are stored into the floating gates of the transistors.

EEPROMs will be specifically considered here, in which the state of any memory cell, or of the floating-gate transistor comprising the cell, can be

15   altered by causing electrons to flow through a thin layer of silicon oxide by tunnel effect.

Description of the Related Art

It is well known to the skilled persons in the art that EEPROMs exist in two main types, i.e., one type having a single polysilicon level provided to form

20   the floating gate region, and another type having two discrete polysilicon levels provided to also form a control gate region. This distinction is, however, irrelevant to this invention.

The individual non-volatile EEPROM cell comprises a FET or a MOSFET transistor having a drain region and a source region. These regions are

25   integrated in a semiconductor substrate and isolated from each other by a substrate portion known as the channel region. A floating gate region is formed above the substrate and is separated from the latter by a thin layer of a dielectric oxide known as the tunnel oxide.

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When the conduction channel of the floating-gate transistor is put in a saturated state, the agitation of the hot carriers (consisting of electrons when the channel is of the N type) releases sufficient energy for them to flow past the barrier formed by the tunnel oxide between the conduction channel and the floating gate.

5   The hot carriers then become trapped within the floating gate.

With a sufficiently high program voltage, the electrons trapped in the floating gate will be unable to leave it, although they keep being agitated. However, this agitation produces inadequate energy for them to get out of the floating gate. As a result, these electrons block the conduction channel with an

10   electric field.

To erase the cell, a high voltage is applied to the drains and sources of the floating-gate transistors , with the floating gate held at a zero potential. Under such conditions, a powerful reverse electric field is created in the transistor, which causes the trapped carriers to migrate toward the drain or the source

15   electrode.

It can be appreciated from the foregoing that, for the purpose of an intensified integration, any reduction in size of these memory cells goes forcibly through a reduction of the coupling surfaces between the floating gates and the conduction channels of the floating-gate transistors. This reduction of the coupling

20   surfaces alters the conditions for conduction by the transistor channel so deeply that the thickness of the tunnel oxide also has to be reduced, down to less than 80 Ångströms (1 Ångström = 0.1 nm).

The thickness of the tunnel oxide turns out to be very difficult to reduce for two reasons. On the one hand, with the decrease of thickness, fault

25   density is bound to increase and the rate of product acceptance decrease. On the other hand, charge (or electron) retention in the floating gates diminishes with reduction in thickness.

In reality, due to their agitation, the electrons do flow at least to some degree past the barrier created by the thick gate oxide. As a result, the information

30   stored in a memory location will vanish gradually. It is presently estimated to

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practically disappear over a 10-year period. If the tunnel oxide were provided at a thinner dimension, this retention time would be greatly shortened.

In order to reduce the dimension of the thin layer of tunnel oxide while retaining its primary dielectric function, other migrating mechanism has been
5 considered whereby the electrons flow along a conduction path other than the dielectric oxide barrier, and become trapped in the floating gate region. For example, as pointed out by D.I. Gittins et al., *Nature*, 11.02.2000, vol. 408, pages 67-69, there exist organic molecules that contain redox centers, *i.e.*, chemical species whose oxidation number (and hence, electron structure) can be modified
10 reversibly. These molecules support a so-called resonant tunneling, and perform promisingly when provided as molecular layers between electric contacts. However, their integration to more complex structures still poses some problems.

Exemplary of such molecules are compounds that contain a reversibly reducible bipyridinium group centrally located, *e.g.*, N,N-di-(10-
15 mercaptodecyl)-4,4'-bipyridinium dibromide.

These compounds usually contain terminal thiol groups in order for them to become bonded to the gold of electrodes used for electrical measuring purposes.

Since it would be extremely difficult to provide gold electrodes in the
20 form of parallel plates spaced one molecule-length (approximately 3 nm) apart, the above molecules are tested by bonding them with one end to one electrode and with the other end to a gold nano-particle (measuring about 6 nm in diameter) that, in turn, is used as a contact of a scanning tunneling microscope operated in an electric-probe mode.

25 While the above-outlined arrangement is useful as far as determining the electrical characteristics of the molecules and controlling the conduction mechanisms and paths (tunneling, resonant tunneling, etc.) is concerned, it is incompatible with silicon-integrated circuits.

Accordingly, there exists in the art a need for methods of integrating
30 molecular layers to conventional silicon-based microelectronic structures and

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enabling them to function as carriers of electrically charged particles. The present invention satisfies this need and provides further related advantages.

BRIEF SUMMARY OF THE INVENTION

One aspect of the present invention is to provide a hybrid
5 configuration in which organic molecules are bonded to conventional silicon-based microelectronic structures and enabling them to function as carriers of electrically charged particles. It was found that the basic component of nearly all integrated electronic circuits, *i.e.*, the MOS or the MOSFET transistor, would meet the requirement of receiving said molecules.

10 In one embodiment, the present invention is related to a method of controlling and modulating the charge flow through a dielectric oxide of a MOS transistor, wherein the transistor structure comprises a layer of silicon oxide (gate oxide) formed between two silicon plates, with the plates overhanging the silicon oxide layer all around to define an undercut having a substantially rectangular
15 cross-sectional shape and a height of about 3 nm, said method comprising the steps of:

chemically altering the surfaces of said silicon plates to have different functional groups in said undercut from those in the remainder of the surfaces; and

20 selectively reacting said functional groups located at the undercut with an organic molecule so as to establish a covalent bond to each of the molecule ends, said molecule containing a reversibly reducible center and having a molecular length of about 3 nm.

said organic molecule has the formula R_1-Y-R_1,
25 wherein,

Y is a redox center having the following formula:

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$$-N^+ \diagup\!\!\!\diagdown\!\!\!\!= \!\!\! \diagup\!\!\!\diagdown N^+-$$

$$2\,Z^-$$
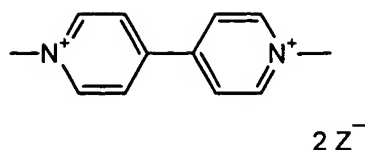
R_1 is a $-CH_2-(CHR_2)_n-R_3$ chain, wherein n=6-8;

R_2 is H or C_1-C_6alkyl group;

R_3 is selected from a group consisting of $-CH_2-CH_2-X$, $-CH=CH_2$, $-C\equiv CH$,

5   and $C\equiv N$, wherein X is either $-SH$ or $-SiH_2Cl$; and

Z^- is a monovalent anion.

       In another embodiment, the instant invention is related to a transistor structure comprising a layer of dielectric silicon oxide formed between two silicon plates, wherein said plates overhang said oxide layer all around to define an

10   undercut having a substantially rectangular cross-sectional shape and a preset height, and wherein the surfaces of said plates at said undercut have different functional groups from those in the other surfaces.

       The features and advantages of the method according to the invention will be apparent from the following description of an embodiment thereof,

15   given by way of example and not of limitation with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

       In the drawings:

       Figure 1 shows schematically a structure of a conventional MOS

20   transistor; and

       Figure 2 is an enlarged detail view of the structure shown in Figure 1 as embodying this invention.

DETAILED DESCRIPTION OF THE INVENTION

This description refers to a storage circuit application for convenience of illustration only, it is possible for the invention to be applied to integrated circuits of any kind that incorporate field-effect transistors.

5   As mentioned above, one aspect of the present invention is to provides a hybrid configuration in which organic molecules are bonded to conventional silicon-based microelectronic structures. It was found that the basic component of nearly all integrated electronic circuits, *i.e.*, the MOS or the MOSFET transistor, are suitable to receive said molecules.

10   A MOS transistor, of which Figure 1 is only an enlarged partial view, is characterized by a structure with parallel layers consisting of a bottom silicon layer 1 and a top silicon layer 2 that are separated by a dielectric oxide layer 3, forming the gate oxide and being about 3 nm thick with the current technology. Layer 1 may be a semiconductor substrate, and layer 2 may be polysilicon.

15   As shown in the drawing, the polysilicon layer 2 overhangs the dielectric oxide layer 3 all around, thereby defining an undercut in cooperation with the substrate 1.

Thus, an undercut 5 of substantially rectangular cross-sectional shape is formed between the peripheral edge of the polysilicon top layer 2 and the 20   substrate 1. It has been thought that the aforementioned organic molecules could fit in this undercut, whose height is controlled by the gate oxidation process to vary between 2 and 100 Ångströms. The layers 1 and 2 will also be referred to as the plates hereinafter.

The molecules should be anchored with one end in the bottom 25   surface 9 of the top silicon layer 2 (polysilicon) and with the other end in the top surface 10 of the bottom silicon layer 1 (the substrate), as in the even more enlarged view of Figure 2.

For the molecules to become anchored, said surfaces should include suitable functional groups to bond to the terminating groups of the molecules. The 30   terminating functional groups of the molecules should be prevented from reacting

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with functional groups in the silicon plate surfaces that lie outside the undercut 5, for otherwise, the molecules would fail to bridge the gap between the plates and function as expected.

Accordingly, the surfaces of the silicon plates 1 and 2 are chemically altered at the undercut 5 to provide them with functional groups 6, 7 selected from a group that consists of -H, -OH, -Au, and $NH_tR(2_{-t})$, where R is a lower alkyl group, preferably C_1-C_4, and t is 0, 1, or 2.

Thus, one aspect of the present invention involves a method of controlling and modulating the charge flow through a dielectric oxide of a MOS transistor, wherein the transistor structure comprises a layer of silicon oxide (gate oxide) formed between two silicon plates, with the plates overhanging the silicon oxide layer all around to define an undercut having a substantially rectangular cross-sectional shape and a height of about 3 nm, said method comprises the steps of:

chemically altering the surfaces of said silicon plates to have different functional groups in said undercut from those in the remainder of the surfaces; and

selectively reacting said functional groups located at the undercut with an organic molecule so as to establish a covalent bond to each of the molecule ends, said molecule containing a reversibly reducible center and having a molecular length of about 3 nm.

said organic molecule has the formula R_1-Y-R_1, wherein,

Y is a redox center having the following formula:
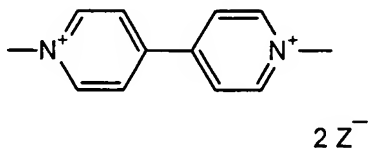
$$-N^{+}\!\!\!\!\diagup\!\!\!\!\bigcirc\!\!\!\!-\!\!\!\!\bigcirc\!\!\!\!N^{+}-\qquad 2\,z^{-}$$

R_1 is a -CH_2-$(CHR_2)_n$-R_3 chain, wherein n=6-8;
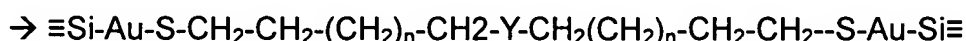
R_2 is H or C_1-C_6 alkyl group;

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R_3 is selected from a group consisting of $-CH_2-CH_2-X$, $-CH=CH_2$, $-C\equiv CH$, and $C\equiv N$, wherein X is either $-SH$ or $-SiH_2Cl$; and

Z^- is a monovalent anion.

In a preferred embodiment, n=7, and more preferred are molecules in which R_2 is H, Z is Br^-, Cl^-, F^-, I^- or PF_6^-, and R_3 is $-CH=CH_2$, $-C\equiv CH$, or $-CH_2-CH_2-SiH_2Cl$.

Molecules in which n=7, R_2 is H, Z^- is Br^-, and R_3 is $-CH_2-CH_2-SiH_2Cl$, $-CH=CH_2$ or $-C\equiv CH$ are most preferred.

The reaction of the functional groups 6, 7 in the surfaces of the silicon plates 1, 2 that define the undercut 5 with an organic molecule 8 of the kind previously described occurs according to one of the following pathways:

$2 \equiv Si-OH + [ClSiH_2-CH_2-CH_2-(CH_2)_n-CH_2]_2Y$

$\rightarrow \equiv Si-O-SiH_2-CH_2-CH_2-(CH_2)_n-CH2-Y-CH_2-(CH_2)_n-CH_2-CH_2-SiH_2-O-Si\equiv$;

$2 \equiv Si-H + [CH_2=CH_2-(CH_2)_n-CH_2]_2Y$

$\rightarrow \equiv Si-CH_2-CH_2 -(CH_2)_n-CH_2-Y-CH_2-(CH_2)_n-CH_2-CH_2-Si\equiv$

$2 \equiv Si-Au + [HS-CH_2-CH_2-(CH_2)_n-CH_2]_2Y$

$\rightarrow \equiv Si-Au-S-CH_2-CH_2-(CH_2)_n-CH2-Y-CH_2(CH_2)_n-CH_2-CH_2--S-Au-Si\equiv$
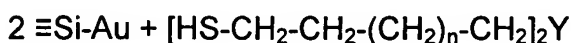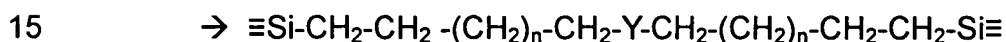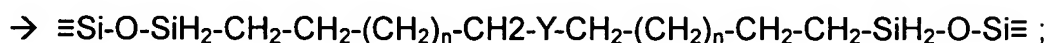
wherein, $\equiv Si$ is the silicon in the surfaces of plates 1, 2, and n and Y have the same meanings as specified above.

The first reaction is widely carried out to substitute $-OCH_3$ groups for the $-OH$ terminations of glass object surfaces in order to make the glass surface hydrophobic that was originally hydrophilic. Such terminations have been used as stoppers in rotaxanes (B. Munn, *The New Chemistry*, ed. N. Hall (Cambridge University Press, Cambridge), 2000, page 375).

The second reaction requires external activation (G.P. Lopinski, D.D.M. Wayner, R.A. Wolkow, *Nature*, 2000, **406**, 48) or a catalyst (F.A. Cotton, G. Wilkinson, *Advanced Inorganic Chemistry*, 5th Ed., 1988, Wiley, New York, page 1255), in the instance of the molecules being short-chained, but takes place

spontaneously in the instance of molecules that, like those used in this invention, have a chain of at least 10 carbon atoms.

Process steps, by which the required transistor structure to implement the method of this invention can be obtained, will now be described in

5   detail.

It is recognized that when the silicon plates in the structure of a MOS transistor are subjected to an etching sequence comprising a first plasma etching step, followed by a wet etching step using aqueous HF, the silicon surfaces emerge from a rinsing step with mixed up $SiH_m(OH)_{n-m}$ terminations, where $n \leq 3$

10   and $m \leq n$ (M. Niwano, J. Kageyama, K. Kinashi, I. Takasashi, and N. Miyamoto, *J. Appl. Phys.*, **76**, 1994, page 2157).

To have the organic molecules anchor themselves as desired in the silicon surface, the terminations in the silicon surface need be controlled.

To obtain surfaces with terminations that are all of the -OH type, wet

15   processing under oxidizing conditions, *e.g.*, treating with $H_2SO_4:H_2O_2$ followed by rinsing with water, can be adopted. This process would leave the silicon surface covered with a highly hydroxylated oxide about the thickness of a single layer.

To obtain surfaces with terminations that are all of the -H type, the native oxide obtained by treating with an aqueous solution of HF may be exposed

20   to a hydrogen atmosphere at moderate temperature for a suitably long time. For example, exposure to H_2 under 30 Pa, at 700°C for 20 minutes, will reduce the amount of oxygen to less than 10^{-2}-single layer (T. Ayoama, K. Goto, T. Yamazaki, and T. Ito, *J. Vac. Sci. Technol.*, A **14**, 1996, page 2909).

The resultant hydrogen-terminated surface is relatively stable, since

25   exposure to air for 10^4 s reveals no appreciable oxidation of the silicon (G.F. Cerofolini, M. Camalleri, C. Galati, S. Lorenti, L. Renna, O. Viscuso, G.G. Condorelli, and I.L. Fragalà, *Appl. Phys. Lett.* **79**, 2001, page 2378).

As said before, the organic molecule should only anchor itself in the undercut region, not all over the surfaces of the individual silicon plates.

Accordingly, the undercut region alone must be provided with suitable terminations for bonding to the molecule.

To achieve this, it has been thought of resorting to anisotropic cathodic sputtering in combination with isotropic wet etching.

The silicon surface of the above MOS transistor structure provided with the undercut is first plasma etched to remove the resist, and then isotropically wet etched using aqueous HF.

At this stage, different procedures will be followed as dictated by the terminating functional groups of the organic molecule that must be bonded in the undercut.

In the instance of molecules that have alkenyl or alkynyl terminations, hydrogen terminations should be provided in the surfaces of the undercut region, and oxygenated terminations in the remaining surfaces of the transistor structure.

In this case, the process comprises the following steps:

1)   exposing the whole structure to hydrogen, at a high temperature (at least 600°C), e.g., at 700°C, under 30 Pa for 20 minutes, so as to cleave all of the -OH terminations and produce a thoroughly hydrogenated surface (see Aoyama et al., above);

2)   removing, by anisotropic sputtering, the hydrogen from the surfaces outside the undercut;

3)   exposing to air, to oxidize the silicon in the sputtered area; and

4)   exposing the transistor structure to a solution of the organic molecule having alkenyl or alkynyl terminating functional groups.

On the other hand, where an organic molecule with chlorosilyl terminating groups is used, hydroxyl terminations should be provided in the surfaces of the undercut region, and hydrogen terminations in the other surfaces.

In this case, the process would include the following steps:

1)   oxidizing under O_2 at a higher temperature than 600°C, e.g., at 800°C, until an oxide thickness same as a single layer is obtained;

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2)	removing, by anisotropic sputtering, the oxygen from the surfaces outside the undercut;

3)	exposing to hydrogen at a high temperature of at least 600°C (exposing at 700°C under 10^{-2} Pa produces hydrogen terminations in the surfaces outside the undercut, and cleaves the siloxane bridges to form hydroxyl terminations in the surfaces of the undercut region (see Aoyama et al., above)); and

4)	exposing to a solution of the organic molecule having chlorosilyl terminating functional groups.

To summarize, the invention teaches fabricating a semiconductor electronic device, specifically a FET or a MOSFET, in which an organic molecule is firmly anchored between two opposite surfaces of an undercut provided between two parallel plates 1, 2 of a conductive material (monocrystalline and polycrystalline silicon), with the plates being separated by a layer 3 of dielectric oxide, e.g., a gate oxide or a tunnel oxide. The organic molecule 8 can be excited electrically as a Schmitt trigger by applying an electric potential thereto.

All of the above U.S. patents, U.S. patent application publications, U.S. patent applications, foreign patents, foreign patent applications and non-patent publications referred to in this specification and/or listed in the Application Data Sheet, are incorporated herein by reference, in their entirety.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.